AKESO ntnb

DESIGN RULE MANUAL // FABRICATION PROTOCOL V1.0

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01 // INTRODUCTION & SCOPE

This document defines the design rules and fabrication constraints for the AKESO ntnb agile micro-fab. All GDSII layouts submitted for fabrication must comply with these specifications to ensure successful high-yield manufacturing of metasurface optical devices.

Our facility specializes in electron-beam lithography (EBL) for ultra-high resolution patterning, combined with ICP-RIE etching for high aspect ratio structures. We support materials including TiO_2, a-Si, Si_3N_4, and various metals.

NOTICE: Designs violating critical constraints will be flagged during DRC and may require re-submission. Contact engineering for feasibility review before submission.

02 // CRITICAL FABRICATION CONSTRAINTS

PARAMETER	VALUE / RANGE	NOTES
Minimum Feature Size (CD) - TiO2	10 nm	EBL process, material dependent
Minimum Feature Size (CD) - Silicon	15 nm	a-Si / c-Si structures
Minimum Gap / Trench Width	15 nm	Aspect ratio restricted
Sidewall Angle	88° - 92°	Optimized for metalens applications
Maximum Etch Depth	1.5 μm	High-selectivity ICP process
Maximum Aspect Ratio	1:15	Depth-to-width ratio
Overlay Accuracy	< 20 nm	EBL multi-layer alignment
Supported Substrate Sizes	1cm² to 4"	Custom shapes supported

CRITICAL: Features below minimum CD or with aspect ratios exceeding 1:15 are subject to process verification. Contact engineering for edge-case feasibility.

03 // LAYER DEFINITIONS & STACK

Standard layer assignments for AKESO ntnb fabrication. Import the accompanying .lyp file for KLayout visualization.

LAYER NAME	GDS LAYER/DATATYPE	MATERIAL	DESCRIPTION
SUBSTRATE	0/0	Fused Silica / Si	Substrate boundary
ALIGN	1/0	Cr/Au	Alignment marks
METAL1	10/0	Ti/Au (5nm/100nm)	Primary metal layer
SIO2	20/0	SiO2 (PECVD)	Dielectric spacer
TIO2_PILLAR	30/0	TiO2 (ALD)	Metasurface pillars
SIN	40/0	Si3N4 (LPCVD)	Silicon nitride layer
ETCH_STOP	50/0	Cr (10nm)	Etch stop layer

LAYER NAME	GDS LAYER/DATATYPE	MATERIAL	DESCRIPTION
AR_COATING	60/0	MgF2/SiO2 Stack	Anti-reflection coating
TEXT	100/0	N/A	Labels and annotations
DRC_EXCLUDE	200/0	N/A	DRC exclusion zones

04 // METASURFACE DESIGN RULES

4.1 TiO2 Nanopillar Arrays (Visible Wavelengths)

RULE ID	DESCRIPTION	MIN	MAX
TIO2.W.1	Pillar width (circular)	10 nm	500 nm
TIO2.S.1	Pillar-to-pillar spacing	15 nm	—
TIO2.H.1	Pillar height	100 nm	1000 nm
TIO2.AR.1	Aspect ratio (H:W)	—	15:1

4.2 Silicon Structures (NIR/IR Wavelengths)

RULE ID	DESCRIPTION	MIN	MAX
SI.W.1	Structure width	15 nm	1000 nm
SI.S.1	Structure spacing	20 nm	—
SI.H.1	Etch depth	50 nm	1500 nm

05 // METAL LAYER RULES

RULE ID	DESCRIPTION	VALUE
MET.W.1	Minimum metal width	50 nm
MET.S.1	Minimum metal spacing	100 nm
MET.E.1	Metal enclosure of via	50 nm
MET.T.1	Maximum metal thickness	500 nm

06 // ETCHING PARAMETERS

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// ICP-RIE TYPICAL PARAMETERS // ═══════════════════════════════════════════════════ PROCESS:
DEEP_SILICON_ETCH ICP_POWER: 800 - 1200 W RF_BIAS: 50 - 150 W PRESSURE: 5 - 15 mTorr
GAS_FLOW: SF6/C4F8 (Bosch) or Cl2/HBr (Continuous) TEMPERATURE: -20°C to +40°C (Cryogenic
available) ETCH_RATE: ~200 nm/min (Si), ~100 nm/min (SiO2) SELECTIVITY: Si:PR > 50:1, Si:SiO2
> 100:1
```

NOTE: Actual etch rates vary with feature density and loading effects. Test structures recommended for process calibration.

07 // ALIGNMENT & OVERLAY

Multi-layer designs require proper alignment mark placement:

- **Global Marks:** Place 4 marks at chip corners, minimum 100 μm from edge
- **Local Marks:** Optional field-level marks for enhanced accuracy
- **Mark Dimensions:** Cross marks 20 μm × 20 μm, line width 2 μm
- **Mark Layer:** Use layer 1/0 (ALIGN)

OVERLAY METRIC	SPECIFICATION
Layer-to-layer overlay (3σ)	< 20 nm
Intra-field stitching	< 10 nm
Global placement accuracy	< 100 nm

08 // SUBSTRATE SPECIFICATIONS

SUBSTRATE TYPE	SIZES AVAILABLE	THICKNESS
Fused Silica	10mm × 10mm to 4" wafer	500 μm - 1 mm
Silicon (100)	10mm × 10mm to 4" wafer	280 μm - 525 μm
Sapphire (C-plane)	10mm × 10mm to 2" wafer	430 μm

SUBSTRATE TYPE	SIZES AVAILABLE	THICKNESS
Glass (Borofloat)	Custom sizes	500 μm - 1.1 mm

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09 // FILE SUBMISSION GUIDELINES

9.1 Accepted File Formats

- **GDSII (.gds, .gds2)** — Preferred format
- **OASIS (.oas)** — For large hierarchical designs
- **STL (.stl)** — For 3D structures (DLW process)

9.2 Submission Checklist

1. Run DRC using provided KLayout script
2. Ensure all layers are correctly assigned per layer map
3. Include alignment marks on layer 1/0
4. Add text labels with chip ID and orientation
5. Define clear die boundaries on layer 101/0
6. Submit via Project Uplink portal: **ntnb.akeso.com.cn/submit**

```
// RECOMMENDED DIRECTORY STRUCTURE // ════════════════════════════════════════════════
project_name/ ├── layout/ │ ├── main_design.gds │ └── test_structures.gds ├── docs/ │ ├──
process_notes.txt │ └── target_specs.pdf └── README.txt
```

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